A SIGNAL DRIVEN LARGE MOS-CAPACITOR CIRCUIT SIMULATOR

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abstract- A software organization of a new circuit simulator, SAMOC (Switched-capacitor Analysis of MOs Circuit) is presented in this paper. SAMOC employs extremely simplified, piecewise linear, resistive models to represent the semiconductor devices such as MOS transistors and ideal diodes in the simulated circuits. SAMOC also supports ideal switches and ideal capacitors for analyzing switched-capacitor networks, which are a weak point in a SPICE simulation. In order to improve the circuit simulation efficiency, circuit partitioning via circuit block extraction is employed by SAMOC. While reading specified devices a posterior-prior relationship is established between each two blocks. SAMOC then creates a block directed graph called signal-block diagram, which can set circuit blocks order for analysis. The DC analysis is accomplished by analyzing all circuit blocks in the order set by the signal-block diagram. An event driven, dynamic simulation, induced by changing the inputs or the internal signals, is performed on the blocks in the path of the signal propagation.

I. Introduction

Simulation of a very large-scale integrated (VLSI) mixed signal circuits has become a mission critical job for computer applications. Advanced semiconductor technologies are capable of producing complex chips and the burden on circuit simulation increases. A more powerful circuit simulation not only demands better computer system with ample and sophisticated resources, but also an efficient simulation engine. In a contemporary circuit simulation system, the computing resources are consumed by evaluating nonlinear device models and solving interconnected circuit equations.

SPICE [1] is a popular, all-purpose circuit simulator, which uses precise device models and sophisticated integration strategy for waveform estimation. SPICE setups the simulation standard in terms of solution accuracy but demands huge system resource for simulating VLSI. Many simulators such as MOTIS[2] SAMSON[3] and SPECS[4] trade precision for a lot faster simulation and use less computing resources. Simplified circuit simulation in these programs employs simplified device models and avoids insignificant changes in the signal value by mean of event-driven simulation. MOTIS employs the event-driven simulation and simplified device model. SAMSON employs the circuit partitioning and event-driven simulation. SPECS employs piecewise constant MOS model. To analyze switched-capacitor networks AWEswit[5] employs capacitor-charge equations instead of KCL and integration techniques for fast simulation.

This paper introduces a circuit simulator program SAMOC (Switched-capacitor Analysis for MOS Circuit) capable of efficient simulation of large analog MOS circuits on a resource limited computer system. SAMOC employs two strategies to improve the simulation efficiency. One is a piecewise linear analysis for analog circuits with MOS

devices in separate current-voltage and charge-voltage modes. The other one is an event driven, block circuit analysis induced by circuit partitioning. The simulator is applicable to large analog systems built predominantly by MOS transistors and linear capacitors. Problem specification is presented in section II. The simplified MOS transistor model is described in section III using piecewise linear approach. Section IV presents the capacitive network analysis and section V presents circuit partitioning and building the signal-block diagram. Section VI illustrates the circuit analysis via signal-block diagram and section VII is the conclusion.

II. Problem specification

Analog MOS circuits are assumed to process two kinds of signals – the current signals which relate currents and voltages, and the charge signals, which relate charges and voltages. Two separate modes of analysis handle these kinds of signals. Resistive analysis (I-V realm analysis) which uses relations between currents and voltages, and charge-voltage analysis (Q-V realm analysis) which uses relations between currents and voltages.

The piecewise linear approach to MOS transistors modeling in SAMOC is based on a voltage controlled resistive model. There are three linear regions, which are controlled by V_{GS} and $V_{DS.}$ The other piecewise linear semiconductor device in SAMOC is an ideal diode. It is modeled by a closed circuit when it conducts and by an open circuit when it is inversely biased. A modified Katzenelson algorithm [7] is applied to find a solution of the piecewise linear system.

SAMOC is equipped with switched-capacitor analysis mechanism that formulates charge-based equations with nonzero initial conditions. Both resistive and capacitive

network analyses are performed by means of the modified nodal analysis (MNA). Current and charge based equations can either appear jointly in the same linearized subsystem or be used separately if the subsystem if composed of resistive or capacitive elements only.

Since the computational complexity of solving a linear system is $O(n^{2.81})$, partitioning a circuit into several blocks and analyzing them separately can decrease the computational effort of circuit simulation, especially for large circuits. SAMOC sets the posterior-prior relationships for block analysis and analyzes blocks individually. By block analysis, SAMOC transfers the device-node problem in circuit simulation into block-signal problem. Smaller number of equations to be solved and fewer linear regions in the Katzenelson algorithm accelerate the circuit simulation. As a result, the computer system can simulate larger circuits. Signal driven simulation is implemented by analyzing triggered blocks only so that analysis of many not active blocks is eliminated.

III. Piecewise Linear Models and Resistive Analysis of Semiconductor Devices

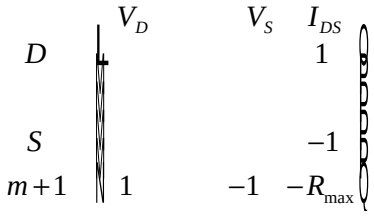
The modified nodal analysis (MNA) which easily models controlled sources and other ideal network elements is employed in SAMOC to perform the resistive analysis. Basic resistive device models are MOS transistors, ideal voltage controlled switches, ideal diodes, and controlled devices. They are either directly described in [Vlach] or can be derived using stamp approach of the MNA. For instance, a piecewise linear resistive model of a MOS transistor is obtained using its linearized equations. The MOS equations used in SAMOC are:

$$I_{DS} = \frac{V_{DS}}{R_{\max}} \qquad V_{GS} \le V_t. \qquad \text{cutoff region}$$

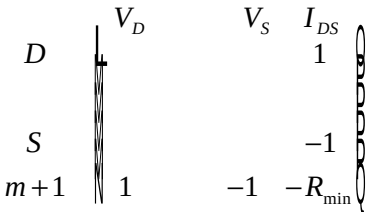
$$I_{DS} = \frac{V_{DS}}{R_{\min}} \qquad \begin{cases} V_{GS} > V_t \\ V_{GS} > \dfrac{V_{DS}(R_{\max} - R_{\min})}{g_m R_{\max} R_{\min}} \end{cases} \qquad \text{linear region}$$

$$I_{DS} = g_m V_{GS} + \frac{V_{DS}}{R_{\max}} \qquad \begin{cases} V_{GS} > V_t \\ V_{GS} < \dfrac{V_{DS}(R_{\max} - R_{\min})}{g_m R_{\max} R_{\min}} \end{cases} \qquad \text{saturation region}$$

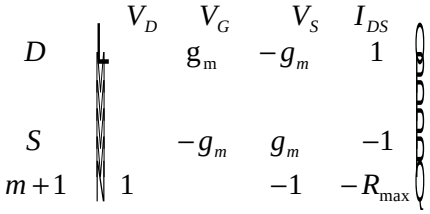
The corresponding device stamps are as follows:

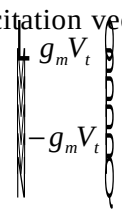


cutoff region



linear region





saturation region

Where parameters used in these models are approximated from:

$$R_{\min} = \frac{1}{b(V_{DD} - V_t)} \quad , \qquad g_m = \frac{0.5}{R_{\min}} \quad , \quad \text{and} \qquad R_{\max} = 1000 \times R_{\min}$$

Where β: MOS transistor gain factor , V_t : the threshold voltage, and V_{DD} : the power supply voltage, and the (m+1)*th* row represents an additional equation dedicated to each MOS transistor.

After device models are put together in the modified nodal equations a piecewise linear analysis is performed using the Katzenelson algorithm. The Katzenelson algorithm simulates circuits with piecewise linear resistive devices, described in their linear regions. A dependent source and a resistive device can model each region. For instance, the voltage controlled piecewise linear resistive device shown in Fig. 1, is characterized by the linear regions shown with the boundaries established by the voltage values … V_{l-1}, V_l, V_{l+1}, ... Katzenelson algorithm adopts an iterative method that begins with an initial guess. A scaling factor *t* must be applied to constrain the new solution to lie inside the linear region *l*, reaching the boundary of one or more regions. SAMOC employs Katzenelson algorithm for analyzing circuits, which contain the piecewise linear devices.

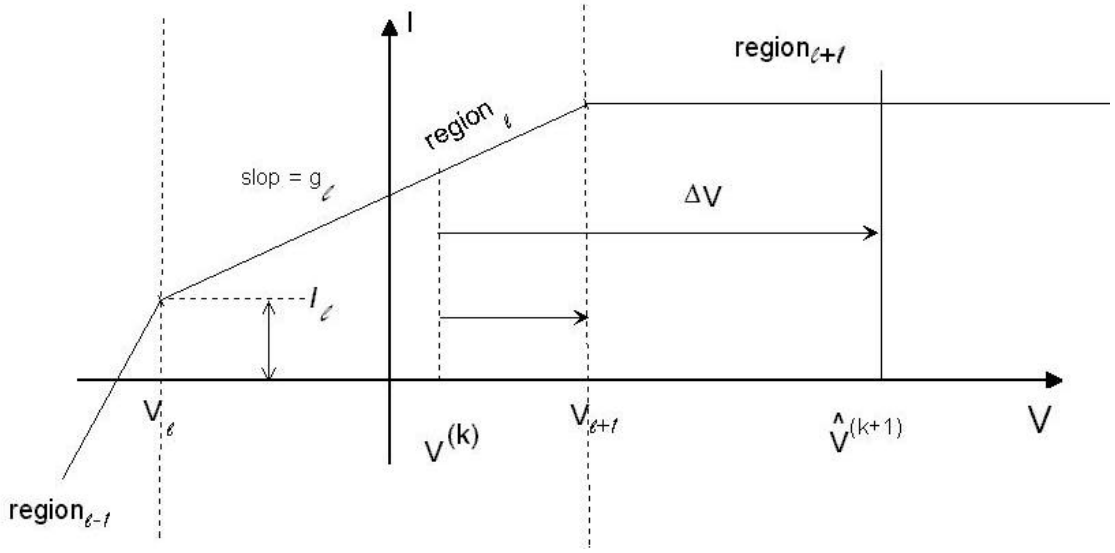


Fig. 1 A voltage controlled resistive device.

MOS transistor state transition

All MOS transistors are in the cutoff state at the beginning of iterations. After the gate to source voltage, V_{GS}, and drain to source voltage V_{DS} are evaluated, the state of the MOS transistor can be determined by:

If $V_{GS} < V_t$, then the MOS transistor is in state 1 (the cutoff region).

If $V_{GS} \geq V_t$ and $V_{GS} > k\ V_{DS}$, then the MOS transistor is in state 2 (the linear region).

If $V_{GS} \geq V_t$ and $V_{GS} < k\ V_{DS}$, then the MOS transistor is in state 3 (the saturation region). V_t is the threshold voltage of the MOS transistor and

$$k = \frac{R_{\max} - R_{\min}}{g_m R_{\max} R_{\min}} \ . \qquad (1)$$

The SAMOC MOS transistor model is represented as a voltage controlled resistive device. The current I_{DS} is a function of V_{DS} and V_{GS} and therefore the evaluation of the scaling factor t is in the 2 dimensional V_{DS} and V_{GS} plain and it is state dependent. The formulas to evaluate t are:

1. In state 1 if $V_{GS} + \Delta V_{GS} > V_t$, then

$$t = \frac{V_t - V_{GS}}{\Delta V_{GS}} \ . \qquad (2)$$

2. In state 2 if $V_{GS} + \Delta V_{GS} < V_t$, then

$$t_1 = \frac{V_t - V_{GS}}{\Delta V_{GS}} \ . \qquad (3)$$

and if $V_{GS} + \Delta V_{GS} < k\,(V_{DS} + \Delta V_{DS})$, then

$$t_2 = \frac{V_{GS} - kV_{DS}}{k\Delta V_{DS} - \Delta V_{GS}} \qquad (4)$$

If both condition (3) and (4) are true, then *t is* the smaller one of t_1 and t_2.

3. In state 3 if $V_{GS} + \Delta V_{GS} < V_t$, then

$$t_1 = \frac{V_t - V_{GS}}{\Delta V_{GS}} \quad . \tag{5}$$

and if $V_{GS} + \Delta V_{GS} < k\,(V_{DS} + \Delta V_{DS})$, then

$$t_2 = \frac{V_{GS} - kV_{DS}}{k\Delta V_{DS} - \Delta V_{GS}} \tag{6}$$

If both condition (5) and (6) are true, then *t is* the smaller one of t_1 and t_2.

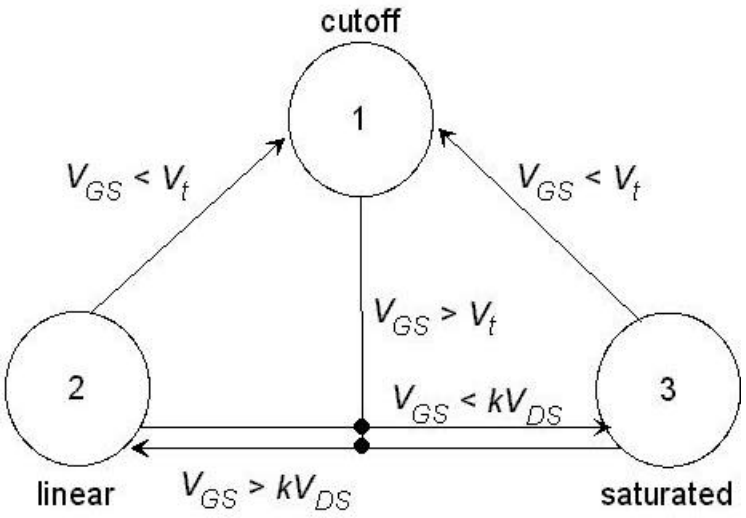


Fig. 2 Dynamic state transition diagram of a MOS transistor.

After the scaling factor *t* is determined by (2)-(6), SAMOC begins to update the states of MOS transistors. The state transition diagram of MOS transistors is illustrated in Fig. 2. A MOS transistor can switch from any state to any other state. Among the possible transitions, checking V_{GS} has higher priority. That is, if previously a MOS transistor was in state 2 and the new V_{GS} is approaching the threshold voltage V_t, $| V_{GS} - V_t | < \varepsilon$, then SAMOC will set the MOS transistor to state 1 without checking the other condition. If $| V_{GS} - V_t | > \varepsilon$ and $| V_{GS} - k\,V_{DS} | < \varepsilon$, then the new state will be 3. The same

situation happens when the MOS transistor is in state 3. SAMOC checks $| V_{GS} - V_t | < \varepsilon$ to determine whether to shift to state 1 or not and then checks $| V_{GS} - k V_{DS} | < \varepsilon$ to determine whether to shift to state 2 or not. On the other hand, if in the previous iteration the MOS transistor was in state 1 and the new V_{GS} is approaching the threshold V_t, $| V_{GS} - V_t | < \varepsilon$, then SAMOC compares V_{GS} and kV_{DS} to determine whether the MOS transistor will shift to state 2 or 3.

A similar analysis of state transition and determination of the scaling factor is conducted in SAMOC for the ideal diode.

IV. Charge-Voltage Network Analysis

The charge-voltage analysis of MOS-capacitor network is based on the matrix equations

$$\boldsymbol{C}\,\boldsymbol{V} = \boldsymbol{W}, \tag{7}$$

where $\boldsymbol{C}$ is the modified capacitive matrix, $\boldsymbol{V}$ is the solution vector and $\boldsymbol{W}$ is the excitation vector. Similar to the MNA in I-V realm, the MNA in Q-V realm is formulated by placing device stamps into $\boldsymbol{C}$ according to the device nodes, parameters and types.

We illustrate the device stamps of Q-V realm analysis on using a linear capacitor. If a capacitor C shown in Fig. 3 has the terminal voltages V_j and $V_{j'}$, then the charges stored at the terminals j and j' are

$$Q_j = C\,(\,V_j - V_{j'}) \tag{8}$$

$$Q_{j'} = C\,(\,V_{j'} - V_j) \tag{9}$$

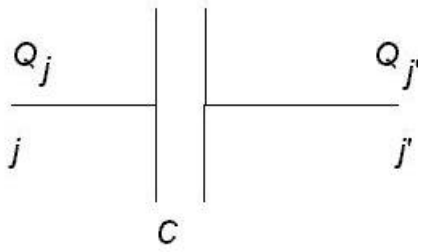


Fig. 3 A capacitor C.

By the law of charge conservation, Q_j and $Q_{j'}$ contributed by C must remain unchanged no matter what was the change of V_j or $V_{j'}$. The device stamp of the capacitor C is

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} j & j' \end{array} \\ \begin{bmatrix} C & -C \\ -C & C \end{bmatrix} \end{array} \qquad \begin{array}{c} \text{excitation vector} \\ \begin{bmatrix} Q_j \\ Q_{j'} \end{bmatrix} \end{array} \quad , \qquad (10)$$

where Q_j and $Q_{j'}$ are evaluated by (8) and (9) respectively. The initial values of V_j and $V_{j'}$ can either be assigned to zero or specified by setting the initial condition.

Many other elements used in the charge-voltage analysis like ideal operational amplifier, ideal switch, ideal diode, voltage source and voltage controlled voltage source have their Q-V realm stamps identical to I-V real stamps with this difference that the corresponding equations describe charges not currents.

In simulation of MOS-capacitor network with ideal diodes and voltage controlled switches, the MNA charge-voltage equations expressed by (7) have to be solved twice. At the first analysis, each ideal diode is treated as an open circuit and switches are set according to initial controlling voltages. Then according to the solution obtained at the first analysis, SAMOC checks the voltages of the two terminals of each ideal diode. If a diode voltage is positive, then the diode is replaced by a short circuit, otherwise that

diode remains open. If any ideal diode was shifted from an open circuit to a short circuit state, then the analysis of (7) has to be repeated.

V. Circuit Partitioning and Signal-Block Diagram

In SAMOC, instead of formulating the MNA equations of the whole circuit, only a portion of the circuit equations are formulated and solved at a time. By employing this method, simulation time is reduced and a lot less memory is required during the circuit simulation. The computational complexity of solving n linear equations is $O(n^{2.81})$. If analyzing a circuit needs n equations, and that circuit can be divided into several blocks which need n_1, $n_{2\ldots}$, equations to solve respectively (where $n = n_1 + n_2 + ...$) then

$$O(n^{2.81}) \geq O(n_1^{2.81}) + O(n_2^{2.81}) + ... \quad (11)$$

After a circuit is partitioned into several blocks, the whole circuit can be analyzed block by block with a significant reduction in the simulation time. Moreover the signal driven approach marks block for analysis only if the input signal changes caused at least one of its devices to change its state. Since in some circuits only a small portion of subcircuits will be activated this will present even greater savings in the simulation effort.

I-V Realm and Q-V Realm Nodes

In SAMOC DC analysis, there are two types of nodes. There are I-V realm nodes and Q-V realm nodes. I-V realm nodes connect with resistive devices. A modified nodal equation based on KCL is formulated at each I-V realm node for all resistive devices connected with that node. Q-V realm nodes, are connected only with capacitors, ideal switches, ideal diodes, ideal OPAMPs, and dependent and independent voltage sources.

A modified nodal equation based on the law of conservation of electrical charge is formulated at each Q-V realm node for all allowed devices connected with that node. In SAMOC analysis, two types of nodes induce two types of circuit formulation methods implemented by different analysis procedures.

I-V Realm and Q-V Realm Circuit Blocks

A circuit block is constructed by a group of circuit devices, which can be analyzed independently from other parts of the simulated circuit. There are two types of circuit blocks: I-V realm and Q-V realm. In an I-V realm block, all devices can conduct DC current; therefore, capacitors are not allowed to appear in these blocks. In SAMOC, I-V realm devices are resistive devices (diodes, resistors, MOS transistors, controlled and independent sources). Capacitors, ideal diodes, ideal switches and voltage sources are categorized as Q-V realm devices and only such devices are allowed in construction of a Q-V realm block. Note that, ideal diodes, ideal switches and voltage sources can appear in both I-V and Q-V realm blocks. Voltage sources are sharable devices and will be discussed in the next section. If an ideal diode or ideal switch connects I-V realm blocks, then it is an I-V realm device. If it connects Q-V realm blocks or an I-V realm block with a Q-V realm block then it is a Q-V realm device.

The resistive network analysis presented in section III is used to analyze the I-V realm blocks, and the MOS-capacitor network analysis from section IV is used to analyze the Q-V realm blocks.

Circuit Block Extraction, Sharable Devices, Sharable Nodes, and Separable Devices

The I-V realm block extraction begins with finding a non-included two-terminal I-V realm device, (most of time, a resistor, a MOS transistor, or an independent current source). I-V realm devices of this kind are usually connected with two I-V nodes and these two nodes are connected with other I-V realm devices. Then these new I-V realm devices are connected with their I-V realm nodes. The I-V realm block extraction procedure continues to include new I-V realm devices and its nodes until no other I-V realm devices are connected to the included nodes. The included nodes and devices have to be marked to prevent infinite loops.

The extraction of Q-V realm blocks is very similar to the extraction of an I-V realm blocks. The extraction begins with finding a capacitor with at least one terminal connected with a Q-V realm node (a node connected only to Q-V realm devices), The appearance of a capacitor can not assure the existence of a Q-V realm block. For example, if a capacitor is connected with two I-V nodes, then there is no conservation of charge equation for that capacitor. That capacitor can be discarded in DC analysis, because it is treated as an open circuit. The Q-V realm node is included into the Q-V realm block and then the incident Q-V realm devices are included. The extraction procedure continues to include Q-V realm devices and their nodes until no other Q-V realm devices are connected to the included nodes.

In the MNA, there is no KCL or charge equation written in a node which connects to a voltage source or to the ground. The voltage value of this type of node is determined before analysis procedure is applied and the amount of current or charge that flows through this node can have any value. The nodes incident to a voltage source can be torn

into many nodes as shown in Fig. 4, without affecting the solution of the MNA applied. This simple resistive network can be divided into two I-V realm blocks by tearing the nodes “1” and “0” into two nodes. So, the independent voltage source V1, and nodes “1” and “0” can belong to both I-V realm blocks. SAMOC defines this kind of nodes as shared nodes and the voltage sources as shareable devices, so that they can be included in different blocks.

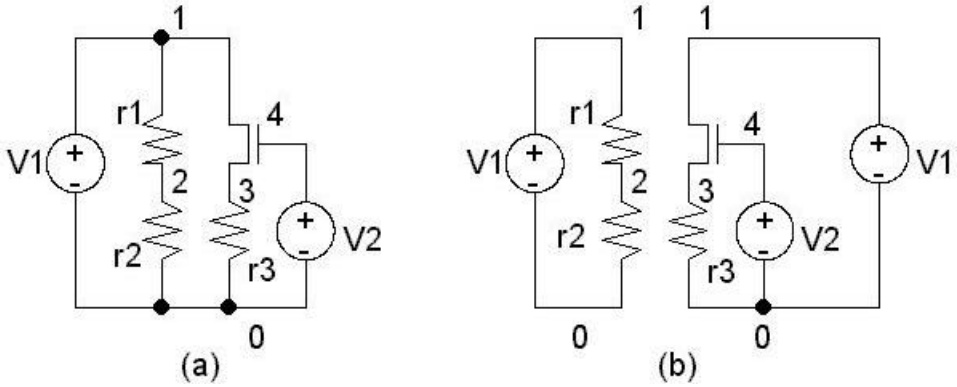


Fig. 4 A node tearing example.

A sharable device is added to a circuit block, which contains both nodes of the sharable device, after the block extraction is completed. The nodes incident to sharable devices are sharable nodes. Sharable nodes can appear in several blocks and no device can be added to a block through a sharable node during the block extraction procedure. Hence, a sharable node establishes the boundary between two blocks.

In addition to the sharable nodes, separable devices can affect a boundary between circuit blocks. A separable device is a device, which does not have a current or charge link between each pair of its nodes. Most of time, separable devices are controlled sources. Their controlling nodes (input) and controlled nodes (output) can

belong to more than one block. MOS transistors are also separable devices in I-V realm block extraction, since there is no DC current from gate to source or from gate to drain.

Posterior-Prior Relationship between Blocks and Signal Block Diagram

A separable device causes posterior-prior relationship in analysis between two blocks. There are two possible situations, which induce a posterior-prior relationship between two blocks:

1. The nodes of a controlled source (or a voltage controlled switch) can belong to different circuit blocks and the block which includes the controlling nodes (input ports) has to be analyzed prior to the block which includes the controlled nodes (output ports).
2. The block containing the gate of a MOS transistor has to be analyzed prior to the block containing the source and gate.

One situation, which might also cause the posterior-prior relationship but is not induced by a separable device, is junction between an I-V realm block and a Q-V realm block. Fig. 5 (a) shows an interface between an I-V block "a" and a Q-V block "b". The voltages in block "b" will not influence the voltages in block "a" in DC analysis, because capacitors are treated as open circuits in DC analysis. However, analyzing block "b" we must know the voltage information from block "a". For this reason, block "a" has to be analyzed prior to block "b".

The posterior-prior relationships between blocks can be represented and stored by creating a directed signal-block graph. In the direct graph representation, the vertices are the blocks and the edges are the signals. The weights of edges are the delay of the

signals. With this signal-block graph, SAMOC can analyze a big circuit block by block transferring signals between them. The resistive network analysis is applied to estimate the behavior of I-V realm blocks, and the charge-voltage network analysis is applied to Q-V realm blocks. The SAMOC analysis not only decreases the required memory in the digital computer system, but is also suitable for parallel processing analysis with multiprocessor architectures.

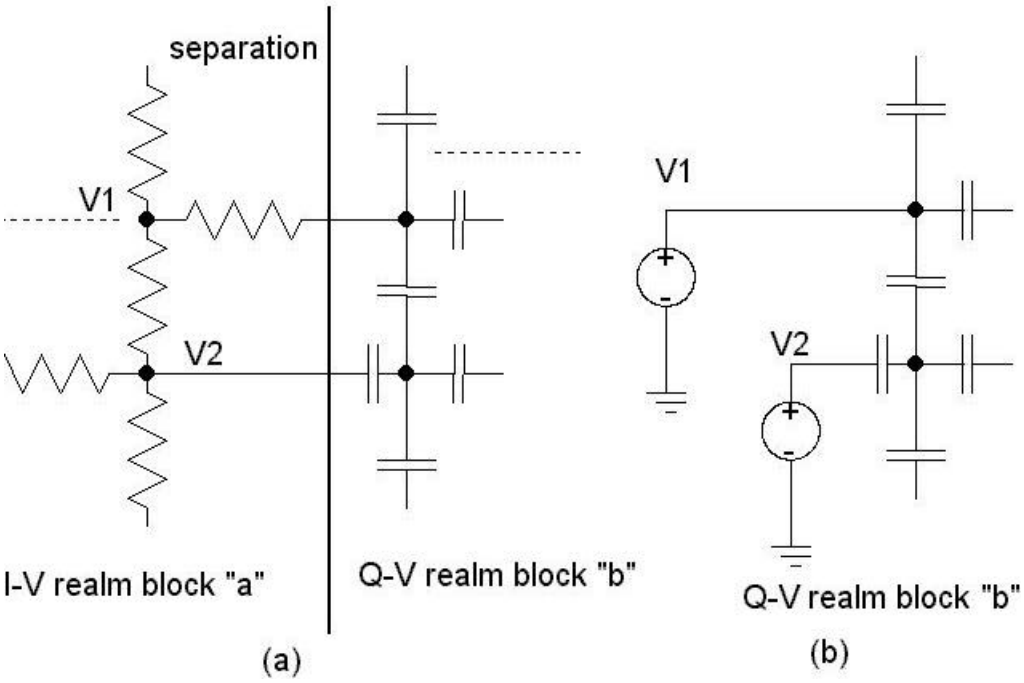


Fig.5 An interface between I-V and Q-V realm blocks.

VI. Circuit Simulation using Signal-Block Diagram

Events between Circuit Blocks

In the signal-block diagram, each block can be analyzed independently from other blocks and has its own solution vector. If the solution vector of a block changes significantly, then this change may induce the necessity to analyze blocks posterior to the one with changed solution vector. The induction of need to analyze consecutive blocks is called an event between blocks. Fig. 6 illustrates a signal-block diagram. A change in the solution vector of block "b" may create events for blocks "c" and "f".

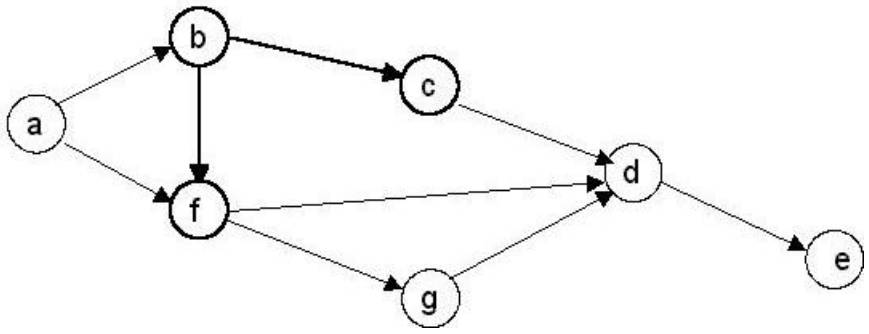


Fig. 6 Events in a signal-block diagram.

Analysis of blocks "f" and "c" may not be necessary depending on the kind of link between blocks. If links are established by controlled sources whose nodes belong to different circuit blocks, or the interface between Q-V block and I-V block, then block "c" and "f" have to be reanalyzed. If a link is established by a voltage controlled switch whose controlling node is in "b" and controlled nodes are in "c" and the on-off state of the switch is not changed, then there is no event in "c". If the link is caused by a MOS

transistor, whose gate is in block "b" and drain and source are in "c" and the change of the solution vector of "b" do not change the transistor state, then there is no event in "c".

DC Analysis

DC analysis of circuit via signal-block diagram requires each block to be analyzed once. The analyzed block may create events for other blocks. SAMOC at first selects all blocks that have events and analyze them until all events are processed. If the circuit has a DC solution, then there is no recursive events between blocks.

Dynamic Analysis Driven by Events

Dynamic analysis caused by time varying excitation vector in SAMOC takes place after the DC analysis. The time varying excitation vector causes the changes of the solution vectors of some blocks that activate other blocks. The dynamic analysis uses the same mechanism as DC analysis.

Computer Implementation of SAMOC and Benchmark Circuit Test

This part will be presented at the final version.

VII. Conclusion

The objective of developing SAMOC is to push the number of simulated devices to the limit of a computer system. This is approached by simplified semiconductor device modeling, Q-V and I-V realm block analysis, and event driven simulation. The simplified semiconductor device models contain piecewise linear resistive model of a MOS transistor and ideal switch model of a diode. A linearized system, needs Katzenelson algorithm to evaluate a solution. A capacitor-charge simulation mechanism is also built in SAMOC to avoid current integration in capacitive devices. The trade-off

is that no transient waveforms are produced. SAMOC is applicable for DC result oriented large analog neural or mixed mode systems with external clock control.

Further computational efficiency improvement in SAMOC is achieved by block analysis based on circuit partitioning of the simulated circuit. Block analysis requires a signal-block diagram, which is built by block extraction and posterior-prior relationship settlement in SAMOC. In analysis an event queue is built to manage and determine with blocks should be analyzed in a given simulation instance.

References

[1] L. W. Nagel and D. O. Pederson, ”Simulation program with integrated circuit emphasis,” in *Proceedings 16th Midwest Symposium Circuit Theory*, Waterloo, Canada, April 1973

[2] B. R. Chawla, *et al*, "MOTIS - An MOS timing simulator," *IEEE Transcations on Circuit and Systems,* vol. CAS-22(12), pp. 901-910, December 1975.

[3] K. A. Sakallah and S. W. Director, " SAMSON2: an event driven VLSI circuit simulator," *IEEE Transactions on Computer-Added Design of ICs and Systems*, vol. 4 pp. 668-684, October 1985.

[4] C. Visweswariah and R. A. Rohrer, "Piecewise approximation circuit simulation," *IEEE Transactions on Computer-Added Design of ICs and Systems,* vol. CAD10, pp. 171-183, February 1991.

[5] R. J. Trihy and R. A. Rohrer, "A switched capacitor circuit simulator: AWEswit," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 217-225, March 1994.

[6] J. Vlach, and K. Singhal, “Computer Methods for Circuit Analysis and Design,**”** Van Nostrand Reinhold, New York 1994

[7] J. Katzenelson, “An algorithm for solving nonlinear resistor networks,” *The Bell System Technical Journal*, vol. 44 pp. 1605-1620, October, 1965.